CUSTOMER APPROVAL SPECIFICATION

( ) Preliminary Specification
(●) Final Specification

Title	PDP60C2#### (60"WXGA PDP MODULE)

Buyer Name	Samplex Electronics Co., LTD	Supplier	LG Electronics Inc.
Model Name		Model Name	PDP60C2####
PART No.		PART No.	

Signature / Date		Signature / Date	
Approved by		Approved by J.S. Kim / Principal Research	
Please return 1 copy for our confirmation with your signature		PDP CM Group, PDP Division, LG Electronics Inc.	

Record of Revisions

Revison No.	Effective Date	Comments
Ver. 1.0	2011. 05. 20	- Establishment
Ver. 1.1	2011. 06. 24	- Establishment
Ver 1.2	2011. 07. 05	- Establishment
Ver 1.3	2011.07.20	- Establishment

CONTENTS

0. Warnings and Cautions

- ✓ WARNING indicates hazards that may lead to death or injury if ignored.
- ✓ CAUTION indicates hazards that may lead to injury or damage to property if ignored.

⚠ WARNING

1) This product uses a high voltage (550 V max.). Do not touch the circuitry of this product with your hands when power is supplied to the product or immediately after turning off the power. Be sure to confirm that the voltage is dropped to a sufficiently low level.

2) Do not supply a voltage higher than that specified to this product. This may damage the product and may cause a fire.

3) Do not use this product in locations where the humidity is extremely high, where it may be splashed with water, or where flammable materials surround it. Do not install or use the product in a location that does no satisfy the specified environmental conditions. This may damage the product and may cause a fire.

4) If a foreign substance (such as water, metal, or liquid) gets inside the product, immediately turn off the power. Continuing to use the products it may cause fire or electric shock.

5) If the product emits smoke, an abnormal smell, or makes an abnormal sound, immediately turn off the power. If noting is displayed or if the display goes out during use, immediately turn off the power. Continuing to use the product as it is may cause fire or electric shock.

6) Do not disconnect or connect the connector while power to the product is on. It takes some time for the voltage to drop to a sufficiently low level after the power has been turned off. Confirm that the voltage has dropped to a safe level before disconnecting or connecting the connector. Otherwise, this may cause fire, electric shock, or malfunction.

7) Do not pull out or insert the power cable from/to an outlet with wet hands. It may cause electric shock.

8) Do not damage or modify the power cable. It may cause fire or electric shock.

9) If the power cable is damaged, or if the connector is loose, do not use the product; otherwise, this can lead to fire or electric shock.

10) If the power connector or the connector of the power cable becomes dirty or dusty, wipe it with a dry cloth. Otherwise, this can lead to fire.

11) This product is designed only for a public display, not for consumer display.

12) Install a protection layer for the viewer safety and the fragile glass product, if it is possible that viewers touch this product directly.

⚠ CAUTION

❑ General

1) Do not place this product in a location that is subject to heavy vibration, or on an unstable surface such as an inclined surface. The product may fall off or fall over, causing injuries.

2) When moving the product, be sure to turn off the power and disconnect all the cables. While moving the product, watch your step. The product may be dropped or fall, leading to injuries of electric shock.

3) Before disconnecting cable from the product, be sure to turn off the power. Be sure to hold the connector when disconnecting cables. Pulling a cable with excessive force may cause the core of the cable to be exposed or break the cable, and this can lead to fire or electric shock.

4) This product should be moved by two or more persons. If one person attempts to carry this product alone, he/she may be injured.

5) This product contains glass. The glass may break, causing injuries, if shock, vibration, heat, or distortion is applied to the product.

6) The temperature of the glass surface of the display may rise to 80°C or more depending on the conditions of use. If you touch the glass inadvertently, you may be burned.

7) Do not poke or strike the glass surface of the display with a hard object. The glass may break or be scratched. If the glass breaks, you may be injured.

8) If you glass surface of the display breaks or is scratched, do not touch the broken pieces or the scratches with bare hands. You may be injured.

9) Do not place an object on the glass surface of the display. The glass may break or be scratched.

❑ Design

1) This product may be damaged if it is subject to excessive stresses (such as excessive voltage, current, or temperature). The absolute maximum ratings specify the limits of these stresses, and system design must ensure that none of the absolute maximum ratings are exceeded.

2) The recommended operating conditions are conditions in which the normal operation of this product is guaranteed. All the rated values of the electrical specifications are guaranteed within these conditions. Always use the product within the range of the recommended operating conditions. Otherwise, the reliability of the product may be degraded. Use of the product with a combination of parameters, conditions, or logic not specified in the specifications of this product is not guaranteed. If intending to use the product in such a way, be sure to consult LGE in advance.

3) This product emits near infrared rays (800 to 1000nm) that may cause the remote controllers of other electric products to malfunction. To avoid this, use an infrared absorption filter and thoroughly evaluate the system and environment.

❑ **Design** (continued)

4) This product uses high-voltage switching and a high –speed clock. A system using this product should be designed so that it does not affect the other systems, and should be thoroughly evaluated.

5) <u>The materials which contain sulfur are forbidden to use, because they may damage PDP module</u>

6) This product has a glass display surface. Design your system so that excessive shock and load are not applied to the glass. Exercise care that the vent at the corner of the glass panel is not damaged. If the glass panel or vent is damaged, the product is inoperable.

7) There are some exposed components on the rear panel of this product. Touching these components may cause an electric shock.

8) This product uses a high voltage. Design your system so that any residual voltage in this product is dissipated quickly when power is turned off, observing the specifications.

9) This product uses heat-emitting components. Take the heat emitted by these components into consideration when designing your system. If the product is used outside the specified temperature range, it may malfunction.

10) This product uses a high voltage and, because of its compact design, components are densely mounted on the circuit board. If dust collects on these components, it can cause short-circuiting between the pins of the components and moisture can cause the insulation between the components to break down, causing the product to malfunction.

11) Regulations and standards on safety and electromagnetic interference differ depending on the country. Design your system in compliance with the regulations and standards of the country for which your system is intended.

12) To obtain approval under certain safety standards (such as UL and EN), a filter that passes a shock test must be fitted over the glass surface of the finished product. In addition, it must be confirmed that the level of UV emissions is within the range specified by such standards.

13) If this product is used as a display board to display a static image, "image sticking" occurs. This means that the luminance of areas of the display that remain lit for a long time drops compared with the luminance of areas that are lit for a shorter time, causing uneven luminance across the display. The degree to which this occurs is in proportion to the luminance at which the display is used. To prevent this phenomenon, therefore, avoid static images as much as possible and design your system so that it is used at a low luminance, by reducing signal level difference between bright area and less bright area through signal processing.

14) Within the warranty period, general faults that occur due to defects in components such as ICs will be rectified by LGE without charge. However, IMAGE STICKING is not included in the warranty. Repairs due to the other faults may be charged for depending on responsibility for the faults.

15) In case of AC PDP driving mechanism, Because the brightness of output is not always proportional to input signals. Therefore the non-linearity of gray can occasionally be observed in certain gray levels as well as Contour and Error Diffusion Noise can be appeared when a dark picture is on the screen especially. These are phenomena that can be observed on the PDP driving mechanism. With simple adjustment to picture brightness control, these can be reduced considerably.

16) Because of the need to control the power consumption on the PDP driving mechanism, the APL(Average Picture Level) mode was equipped. Thus, as the picture on the screen changes, there can be slightly switched in brightness. This also is a phenomenon that can be observed on the PDP driving mechanism.

17) This product is designed to LGE's "Standard" quality grade. If you wish to use the product for applications outside the scope of the "Standard" quality grade, be sure to consult LGE in advance to assess the technological feasibility before starting to design your system.

❑ USE

1) Because this product uses a high voltage, connecting or disconnecting the connectors while power is supplied to the product may cause malfunctioning. Never connect or disconnect the connectors while the power is on. Immediately after power has been turned off, a residual voltage remains in the product. Be sure to confirm that the voltage has dropped to a sufficiently low level.

2) Watching the display for a long time can tire the eyes. Take a break at appropriate intervals.

3) PDP 's brightness and contrast ratio is lower than that of the CRT. The picture is dimmer with surrounding light and better for viewing in dark condition.

4) Do not cover or wrap the product with a cloth or other covering while power is supplied to the product.

5) Before turning on power to the product, check the wiring of the product and confirm that the supply voltage is within the rated voltage range. If the wiring is wrong or if a voltage outside the rated range is applied, the product may malfunction or be damaged.

6) Do not store this product in a location where temperature and humidity are high. This may cause the product to malfunction. Because this product uses a discharge phenomenon, it may take time to light (operation may be delayed) when the product is used after it has been stored for a long time. In this case, it is recommended to light all cells for about 2hours (aging).

7) If the glass surface of the display becomes dirty, wipe it with a soft cloth moistened with a neutral detergent. Do not use acidic or alkaline liquids, or organic solvents.

8) Do not tilt or turn upside down while the module package is carried, the product may be damaged.

9) This product is made from various materials such as glass, metal, and plastic. When discarding it, be sure to contact a professional waste disposal operator.

❑ Repair and Maintenance

Because this product combines the display panel and driver circuits in a single module, it cannot be repaired or maintained at user's office or plant. Arrangements for maintenance and repair will be determined later.

❑ Others

1) If your system requires the user to observe any particular precautions, in addition to the above warnings and cautions, include such caution and warning statements in the manual for your system.

2) If you have any questions concerning design, such as on housing, storage, or operating environment, consult LGE in advance.

1. GENERAL DESCRIPTION

❑ DESCRIPTION

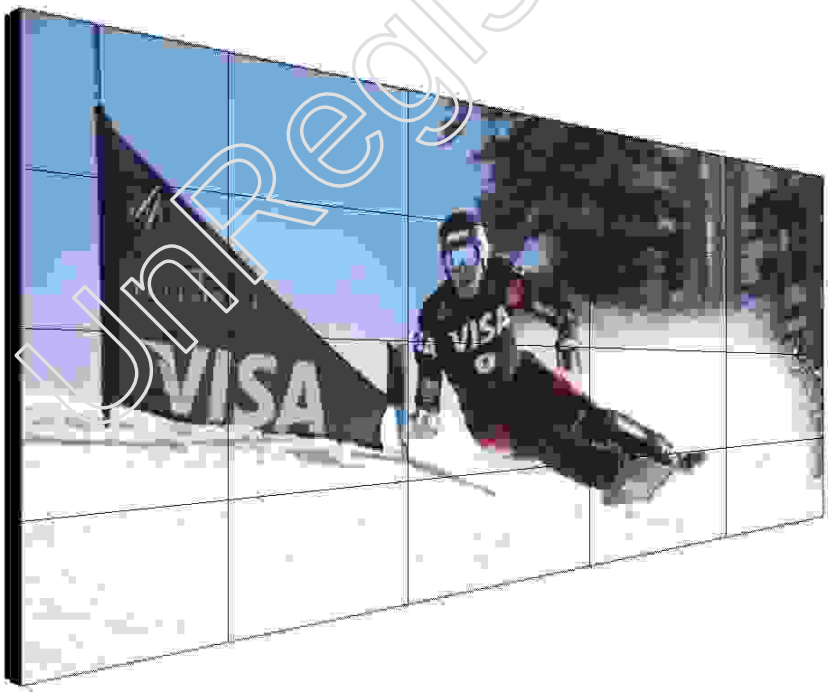
The PDP60C2#### is a 60-inch 16:9 color plasma display module with resolution of 1365(H) × 768(V) pixels. This is the display device which offers vivid colors with adopting AC plasma technology by LG Electronics Inc.

❑ FEATURES

High peak brightness (1,700cd/m2 Typical) and high contrast ratio (1,000,000:1 Typical) enables user to create high performance PDP SETs.

❑ APPLICATIONS

- ✓ Public information display
- ✓ Video conference systems
- ✓ Education and training systems



(Image)

❑ ELECTRICAL INTERFACE OF PLASMA DISPLAY

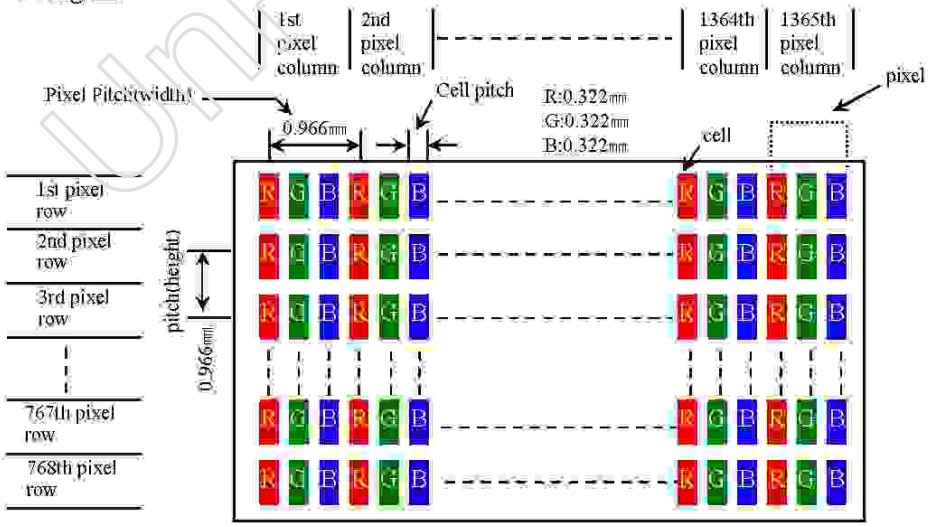
The PDP60C2#### requires only 8/10/12 bits of digital video signals for each RGB color.
In addition to the video signals, six different DC voltages are required to operate the display.
The PDP60C2#### for a multi-vision display is equipped with the AC plasma technology which provides a vivid and natural picture quality.

❑ GENERAL SPECFICATIONS

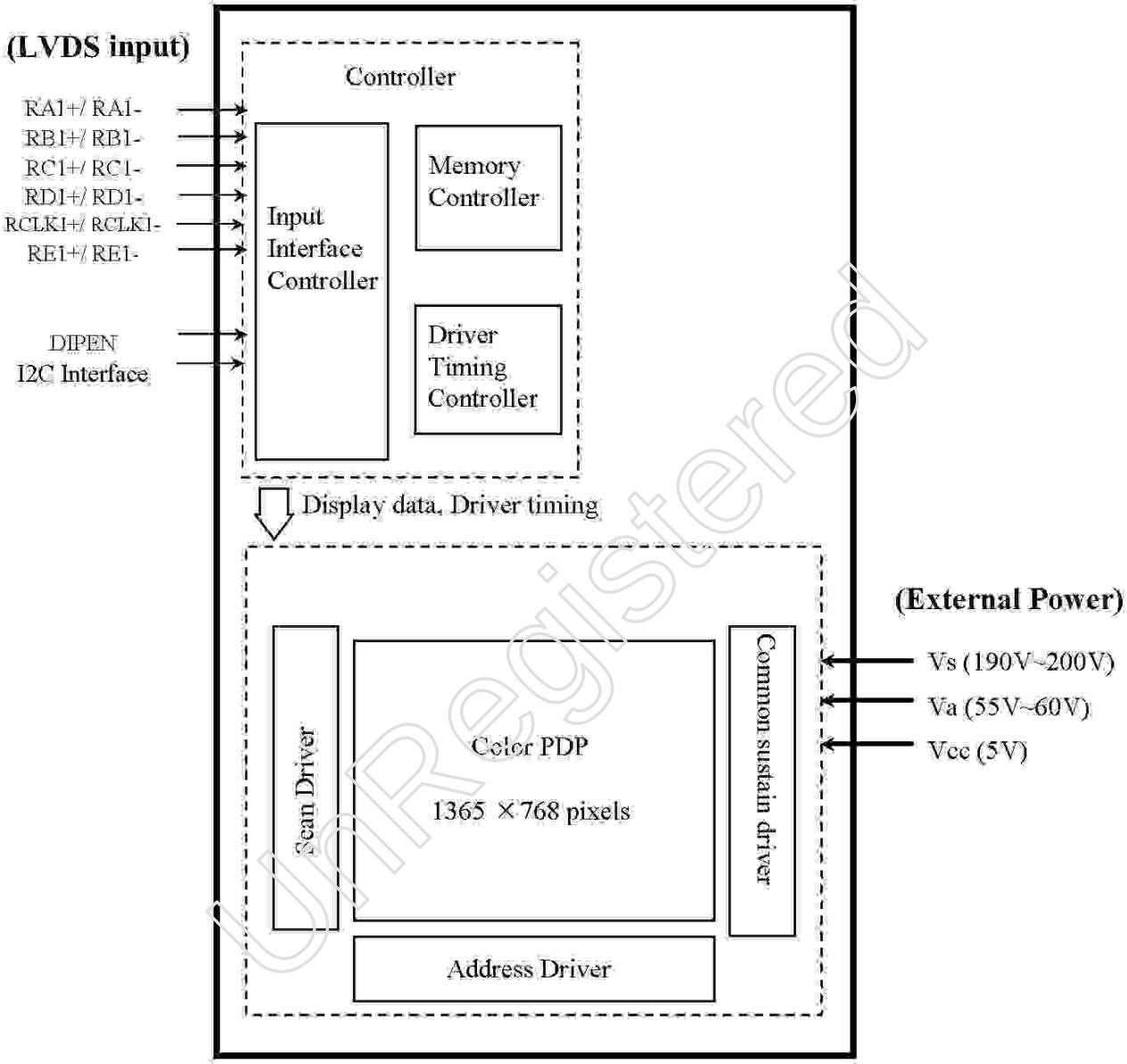
✓ Model Name	: PDP60C2#### (60C2 Model)
✓ Number of Pixels	: 1365(H) × 768(V) (1pixel=3 RGB cells)
✓ Pixel Pitch	: 966㎛ (H) × 966㎛ (V)
✓ Cell Pitch	: 322㎛ (H) × 966㎛ (V) (Green Cell basis)
✓ Seam Size(*)	: 1.5mm (Maximum)
✓ Display Area	: 1318.6(H) × 741.9(V) ± 0.5mm
✓ Outline Dimension	: 1322.3(H) x 745.7(V) x 67.7 (D) ±1 (mm)
✓ Pixel Type	: RGB Closed (Well) type
✓ Number of Gradations	: 12bit (R) 4,096 × (G) 4,096 × (B) 4,096 colors (68.719 billion) : 10bit (R) 1,024 × (G) 1,024 × (B) 1,024 colors (1.073 billion) : 8bit (R) 256 × (G) 256 × (B) 256 colors (16.78 million)
Weight	: 24.2±1 Kg : Net (With PSU), 22.1±1Kg (Without PSU)
✓ Aspect Ratio	: 16:9
✓ Peak Brightness	: Typical 1,700cd/㎡ (1/100 White Window pattern at center, without Filter)
✓ Contrast Ratio	: Average 125:1 (In a bright room with 100Lux at center) : Typical 1,000,000:1 (In a dark room 1/100 White Window pattern at center)
✓ Power Consumption	: Typ. 450 W (Full-White)
✓ Expected Life-time	: Warranty life time 60,000 Hours with continuous operation

☞ Warranty life-time is defined as the time when the brightness level becomes half of its initial value.
* The seam size is described as the width of one side to be connected with other panels.

✓ Display Dot Diagram



❑ BLOCK DIAGRAM



☞ Applied Voltage level is specified at the time when Full-White pattern is displayed on the panel

❑ CONDITIONS OF ACCEPTABILITY

➢ Main Power supply

In order to supply the main power, the manufacturer of end-user products should adopt suitable Main SMPS, DC/DC Converter which are equipped with OCP and OVP.
These characteristics of OCP and OVP should be as follows.

POINT	+ 5V	Va	Vs
OCP	6.0 ~ 15.0	2.3 ~ 4.5	2.3 ~ 4.3
OVP	5.3 ~ 7.0	68 ~ 75	205 ~ 230

- OCP (Over current protection) : This functions to protect power supply or load from output current applied in excess of limited value.
- OVP (Over voltage protection) : This functions to protect against output voltage exceeding a fixed value and against over voltage load.

➢ Insulation

- In order to use information technology equipment or audio/video apparatus, the end-user product should satisfy the insulation and material requirements on Safety Standards of IEC 60950-1, EN 60950-1, UL60950-1 and CSA C22.2 No. 60950-1, or IEC 60065, EN 60065, UL 6500 and CAN/CSA-E60065(CSA C22.2 No. 60065)

➢ Additional requirements

- Proper fire enclosure
- Proper mechanical enclosure
- safety test including Power Supply Board should be preformed as a part of the end-user product investigation.

2. ELECTRICAL SPECIFICATIONS

❑ Absolute Power Specifications

Item	Symbol	Condition	Min.	Max.	Unit	Remarks
Logic Voltage	Vcc	25°C	4.5	6	V	
Address Voltage	Va	25°C	—	65	V	
Sustain Voltage	Vs	25°C	—	215	V	

❑ Input Power Specifications

➢ Logic Power Supply (Vcc)

Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	4.75	5.0	5.25	V
Voltage Stability		—	—	±5.0	%
Average Current		0.1	—	5	Amean
Voltage Regulation	At the peak current	—	—	30	mVp-p
Ripple & Noise		—	—	300	mVp-p

➢ Address Power Supply(Va)

Item	Condition & Remarks	Min	Typ	Max	Unit
Adjustable Range	Dependent on the characteristics of each PDP	55	—	60	V
Voltage Stability	-	—	—	±1.5	%
Average Current	Variable with the image	0.01	—	2.5	Amean
Ripple & Noise	-	—	—	300	mVp-p

☞ Max current of Va is measured when 2-dot ON/OFF pattern is displayed.

➢ Sustain Power Supply(Vs)

Item	Condition	Min.	Typ	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	190	—	200	V
Voltage Stability	-	—	—	±1.0	%
Peak Current	-	—	—	30	A
Average Current	Dependent on the characteristics of each PDP	0.1	—	2.6	Amean
Voltage Regulation	At the peak current	—	—	3	V
Ripple & Noise	-	—	—	500	mVp-p

☞ Voltage should be set to a specified value which is indicated on the label attached to the module.

❑ Input Power Specifications (Continued)

➢ Writing Scan Bias Power Supply (-Vy)

Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	-195	-190	-189	V
Voltage Stability	-	-	-	±2.0	%
Average Current	-	1	-	100	mA
Voltage Regulation	At the peak current	-	-	2	V
Ripple & Noise	-	-	-	500	mVp-p

➢ Scan Power Supply (Vsc)

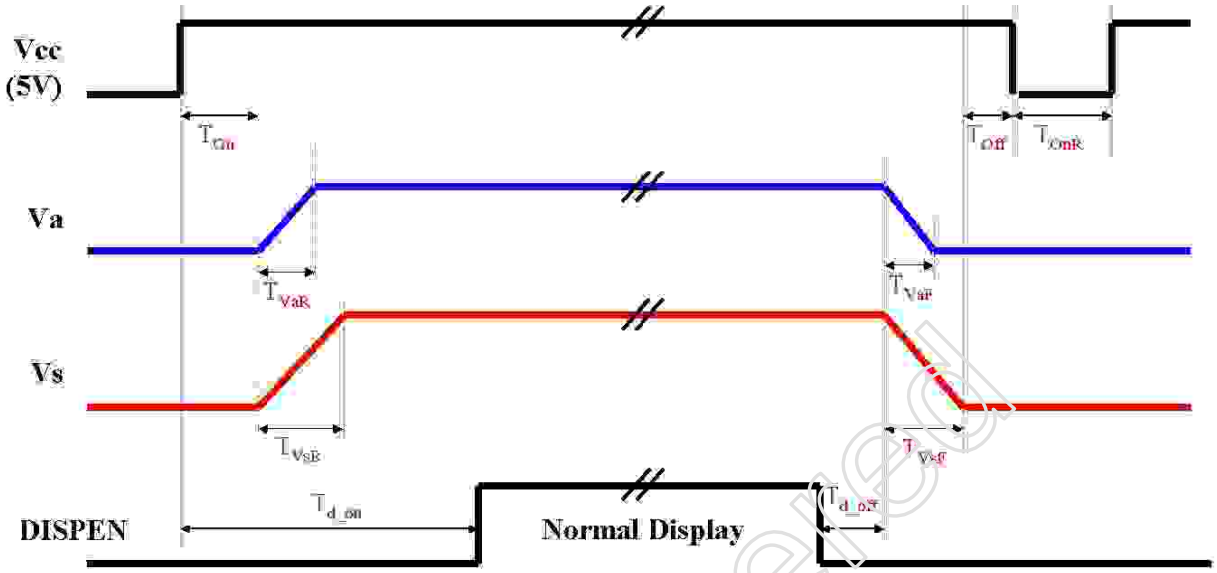
Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	139	140	141	V
Voltage Stability	-	-	-	±1.0	%
Average Current	-	1	-	80	mA
Voltage Regulation	At the peak current	-	-	5	V
Ripple & Noise	-	-	-	500	mVp-p

➢ Z-bias Power Supply (Vzb)

Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	60	67	85	V
Voltage Stability	-	-	-	±1.0	%
Average Current	-	1	-	250	mA
Voltage Regulation	At the peak current	-	-	5	V
Ripple & Noise	-	-	-	500	mVp-p

☞ Voltage should be set to a specified value which is indicated on the label attached to the module.

❑ Power Supply Sequence



Symbol	Description	Min.	Max.	unit
T_{On}	Time interval between 90% of Vcc and 10% of Vs when Power On	750	1250	msec
T_{Off}	Time interval between 10% of Vs and 90% of Vcc when Power Off	20	-	msec
T_{OnR}	Time interval between 10% of Vcc and 90% of Vcc when Power On	2000	-	msec
T_{VaR}	Rising Time of Va (10% to 90%)	10	300	msec
T_{VaF}	Falling Time of Va (90% to 10%)	50	500	msec
T_{VsR}	Rising Time of Vs (10% to 90%)	100	500	msec
T_{VsF}	Falling Time of Vs (90% to 10%)	90	500	msec
T_{d_on}	Time interval between 90% of Vs and DISPEN rising edge when Power On	3100	-	msec
T_{d_off}	Time interval between DISPEN falling edge and 90% of Vs when Power Off	1500	6000	msec
		Recommended 2sec		

☞ *) If power sequence does not meet to above sequence diagram, PDP drivers may be damaged permanently.

☞ Vcc should be lower than 0.1V when turn on just after turn off.

☞ Even when AC input power supply is switched ON/OFF, above sequence should be observed strictly.

❑ LVDS Signal and LVDS Receiver

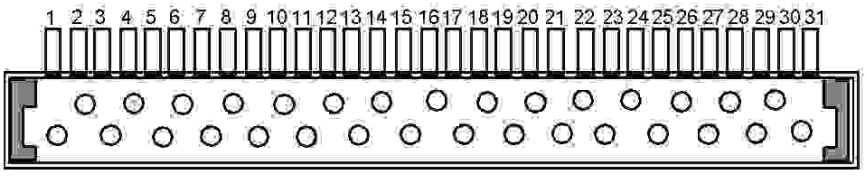
➢ Definitions and Functions of LVDS Signal

Symbol	Function and Description
RA+	Channel A Pos. Receiver Input
RA−	Channel A Neg. Receiver Input
RB+	Channel B Pos. Receiver Input
RB−	Channel B Neg. Receiver Input
RC+	Channel C Pos. Receiver Input
RC−	Channel C Neg. Receiver Input
RD+	Channel D Pos. Receiver Input
RD−	Channel D Neg. Receiver Input
RE+	Channel E Pos. Receiver Input
RE−	Channel E Neg. Receiver Input
RCLK+	CLK Pos. Receiver Input
RCLK−	CLK Neg. Receiver Input

➢ Video Input Connector (P321)

Connector Type : C-NET, 1001-65131 31P

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	
1	GND	11	RD1-	21	NC	
2	RA1-	12	RD1+	22	NC	
3	RA1+	13	GND	23	NC	
4	RB1-	14	GND	24	RE1-	
5	RB1+	15	NC	25	RE1+	
6	GND	16	NC	26	GND	
7	RC1-	17	NC	27	DISPEN	3.3V level
8	RC1+	18	NC	28	I²C SDATA	3.3V level
9	RCLK1-	19	GND	29	I²C SCLK	3.3V level
10	RCLK1+	20	NC	30	NC	
				31	GND	



C-NET 1001-65131 31P pin number (Top view)

☞ substitute JAE, FI-TWEP31-VF

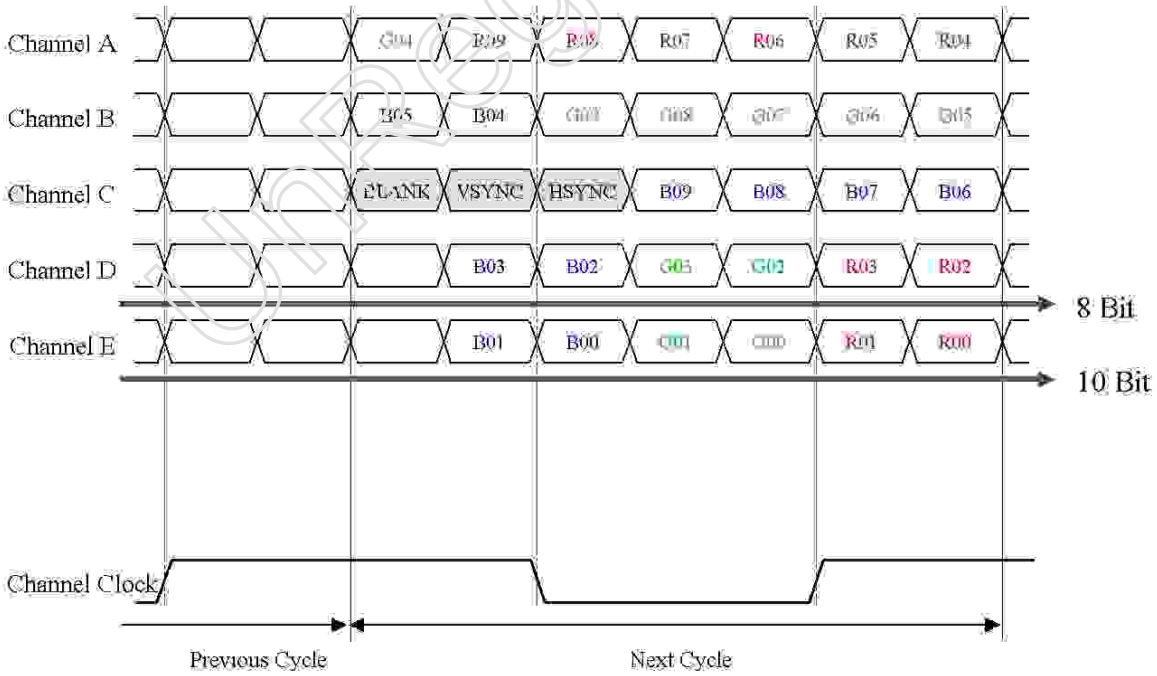
❑ LVDS Signal and LVDS Receiver (continued)

➢ Output Signals of LVDS Receiver

Symbol	Function and Description
R9 ~ R0	14-bit Red Pixel video signal (R9 : MSB, R0 : LSB)
G9 ~ G0	14-bit Green Pixel video signal (G9 : MSB, G0 : LSB)
B9 ~ B0	14-bit Blue Pixel video signal (B9 : MSB, B0 : LSB)
PIX_CLK	Clock Signal which synchronous to video signal
$\overline{\text{Vsync}}$	vertical synchronous signal
$\overline{\text{Hsync}}$	horizontal synchronous signal
$\overline{\text{BLANK}}$	'HIGH' level : data is valid 'LOW' level : data is invalid
DISPEN	'HIGH' level : Display Enable 'LOW' level : Non Display

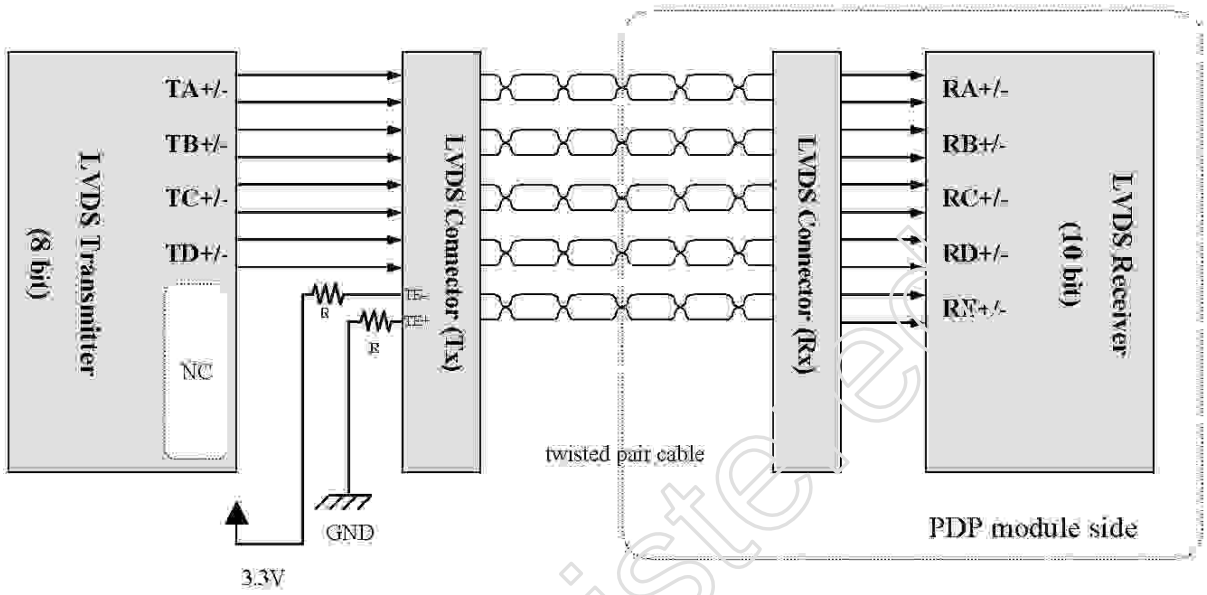
☞ Each of the RGB signals can be changed with the Gamma Mode.
☞ You should not adjust any inverse gamma compensation. Because the inverse gamma compensation is adjusted in the PDP side already.
☞ In preparing the LDVS signal cable, The twisted pair cable should be used for the differential signal.

➢LVDS Receiver IP mapping [10bit]



❑ LVDS Signal and LVDS Receiver (continued)

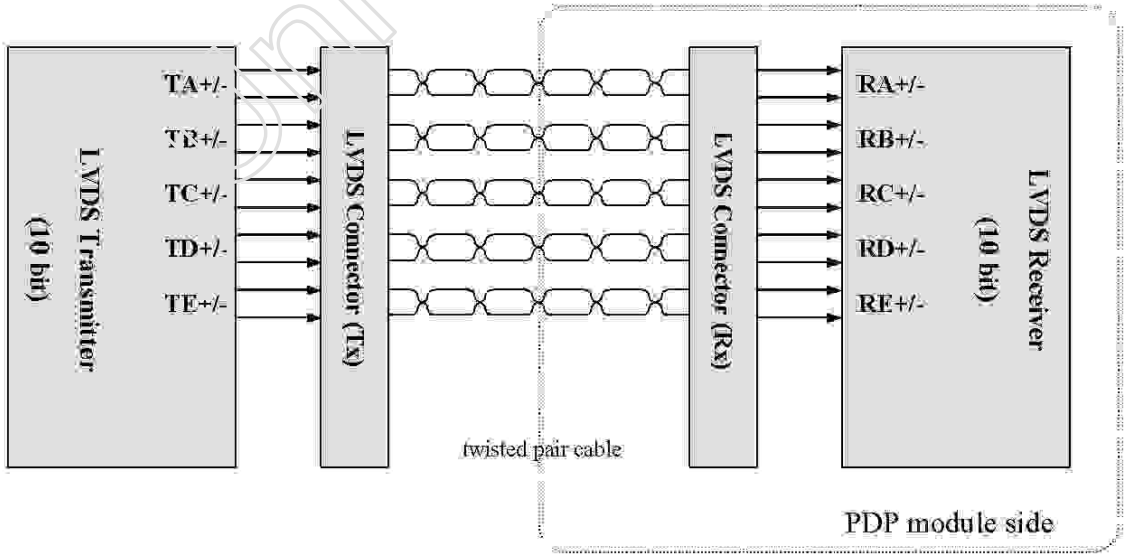
➢ 8bit application [10bit application]



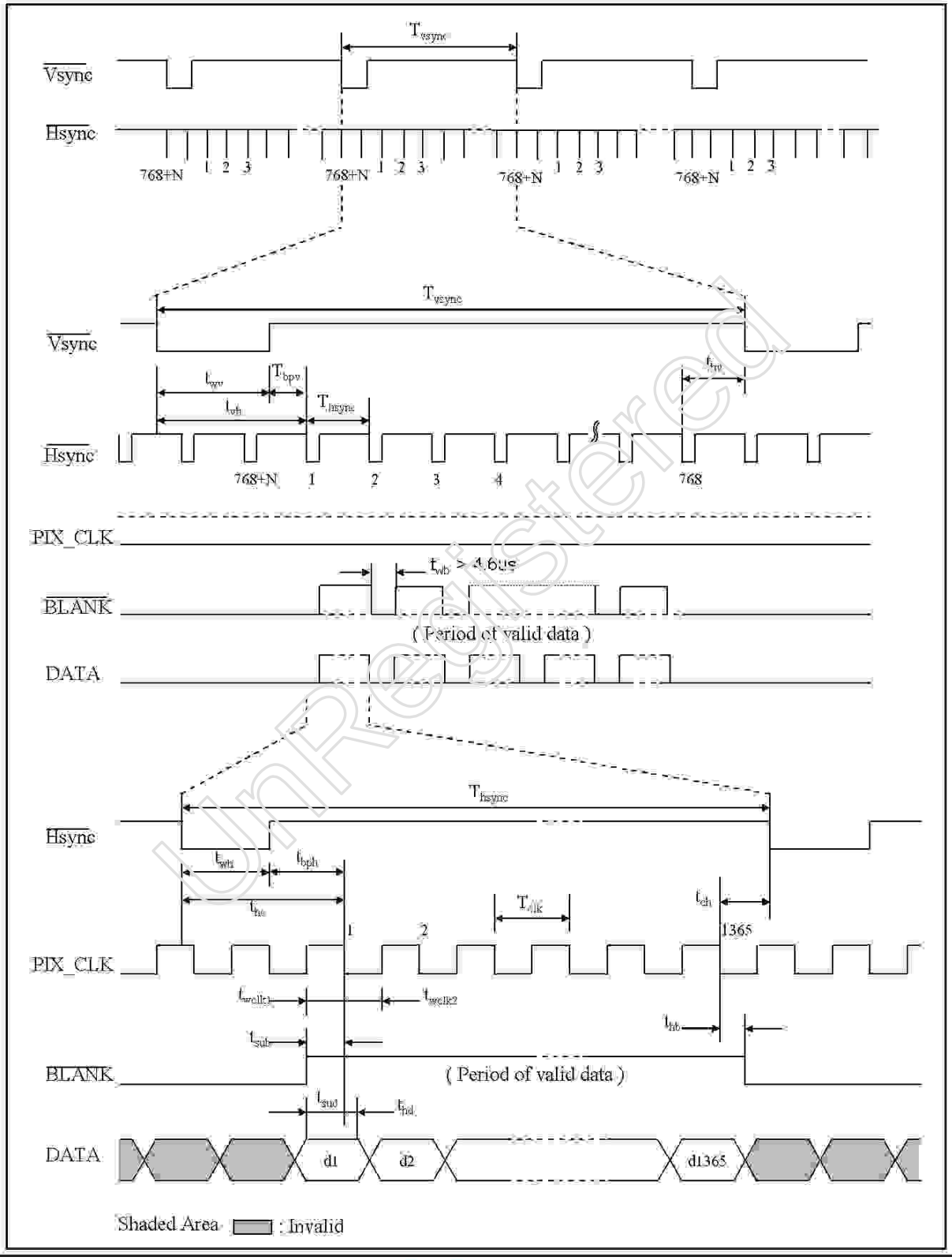
☞ To use (only) 8bit video signal, "TE+" is to be tied to ground signal and "TE-" is to be tied to 3.3V signal. (to set the 2 LSB of 10 bits video signal to "0(LOW)") The value of resistor, R is recommended 10 KΩ resistance.)

☞ In the case of 10 bit video signal, the connector pin without a video signal should be '0(LOW)'.

➢ 10bit application



❑ Input Signal Timing Diagram (Non-interlaced Mode)



❑ Input Signal Timing Specification

➢ 60Hz Mode

No.	Symbol	Min	Typ	Max.	Unit	Remark
1	T_{vsync}	16.528 (795H)	16.674 (802H)	16.794 (808H)	ms (H)	1 frame (Typ.) = 59.53~60.50Hz
2	t_{wv}	62.37 (3H)	83.16 (4H)	103.95 (5H)	μs (H)	
3	t_{vh}	374.22(18H)	395(19H)	415.8(20H)	μs (H)	
4	t_{hv}	-	311.85(15H)	-	μs (H)	
5	T_{hsync}	20.763 (1540D)	20.790 (1542D)	20.844 (1546D)	μs (D)	1D=13.4825ns
6	t_{wh}	0.135 (10D)	0.162 (12D)	0.189 (14D)	μs (D)	
7	t_{hc}	1.591 (118D)	1.618 (120D)	1.645 (122D)	μs (D)	
8	t_{ch}		0.755 (56D)		μs (D)	
9	t_{clk}	13.2785 (75.31MHz)	13.4825 (74.170MHz)	14.0 (71.429MHz)	ns	
10	t_{wclk1}		6.7412		ns	
11	t_{wclk2}		6.7412		ns	
12	t_{sub}		6		ns	$t_{sub} \leq t_{hc}$
13	t_{hb}		5		ns	$t_{hb} \leq t_{ch}$
14	t_{sud}		6		ns	
15	t_{hd}		5		ns	

☞ Min. & Max. of each signal is measured value when other signal is Typ.

☞ Tvh (Vertical Front Porch) ≥ 4H

☞ Tvh (Vertical sync width + Vertical Back Porch) ≥ 15H

❑ Input Signal Timing Specification (Continued)

➢ 50Hz Mode

No.	Symbol	Min	Typ	Max.	Unit	Remark
1	T_{vsync}	19.792 (952H)	19.958 (960H)	20.207 (972H)	ms (H)	1 frame = 50.11Hz
2	t_{wv}	187(9H)	208(10H)	229(11H)	μs (H)	
3	t_{vh}	520(25H)	541(26H)	561(27H)	μs (H)	
4	t_{hv}	-	3.45(166H)	-	μs (H)	
5	T_{hsync}	20.763(1540D)	20.790(1542D)	20.844(1546D)	μs (D)	1D=13.4825ns
6	t_{wh}	0.135(10D)	0.162(12D)	0.189(14D)	μs (D)	
7	t_{hc}	1.591(118D)	1.618(120D)	1.645(122D)	μs (D)	
8	t_{ch}	-	0.755(56D)	-	μs (D)	
9	t_{clk}	13.342 (74.95MHz)	13.4825 (74.170MHz)	14 (71.429MHz)	ns	
10	t_{wclk1}	-	6.7412	-	ns	
11	t_{wclk2}	-	6.7412	-	ns	
12	t_{sub}	-	6	-	ns	$t_{sub} \leq t_{hc}$
13	t_{hb}	-	5	-	ns	$t_{hb} \leq t_{ch}$
14	t_{sud}	-	6	-	ns	
15	t_{hd}	-	5	-	ns	

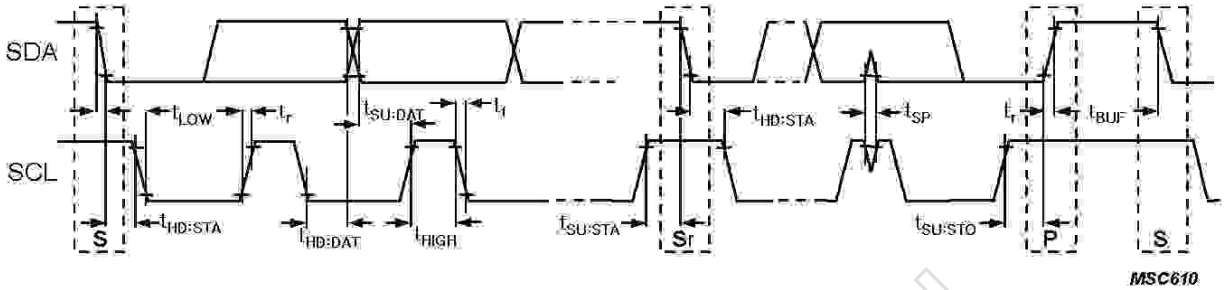
☞ Min. & Max. of each signal is measured value when other signal is Typ.

☞ Thv (Vertical Front Porch) ≥ 4H

☞ Tvh (Vertical sync width + Vertical Back Porch) ≥ 15H

❑ I²C Timing Specification

➢ I²C Timing Diagram



MSC610

➢ I²C Timing Specification (Characteristics of the SDA and SCL bus lines)

PARAMETER	SYMBOL	STANDARD-MODE		UNIT
		MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	kHz
Hold time (repeated) START condition After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$			µs
Data hold time: for CBUS compatible masters for I²C bus devices	$t_{HD;DAT}$	 5.0 0[2]	 - 3.45[3]	 µs µs
DATA Set-up time	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals	t_r	-	1000	ns
Fall time of both SDA and SCL signals	t_f			ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	µs
Capacitive load for each bus line	C_b	-	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	-	V
Noise margin at the High level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	-	V

Notes
1. All values referred to V_{IHmin} and V_{ILmax} levels.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table 6 are allowed.

※n/a = not applicable

❑ I²C Timing Specification

➢ I²C Timing Specification (Characteristics of the SDA and SCL I/O stages)

PARAMETER	SYMBOL	STANDARD-MODE		UNIT
		MIN.	MAX.	
LOW level input voltage: fixed input levels VDD-related input levels	VIL -0.5 -0.5		1.5 0.3VDD	V V
HIGH level input voltage: fixed input levels VDD-related input levels	VIH 3.0 0.7VDD		(2) (2)	V V
Hysteresis of Schmit trigger inputs: VDD > 2V VDD < 2V	Vhys n/a n/a		n/a n/a	V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: VDD > 2V VDD < 2V	 VOL1 VOL3	 0 n/a	 0.4 n/a	 V V
Out fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 pF	Tof	-	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	tSP	n/a	n/a	ns
Input current each I/O pin with an input voltage between 0.1 VDD and 0.9VDDmax	Ii	-10	10	MA
Capacitance for each I/O pin	Ci	-	10	pF

Notes

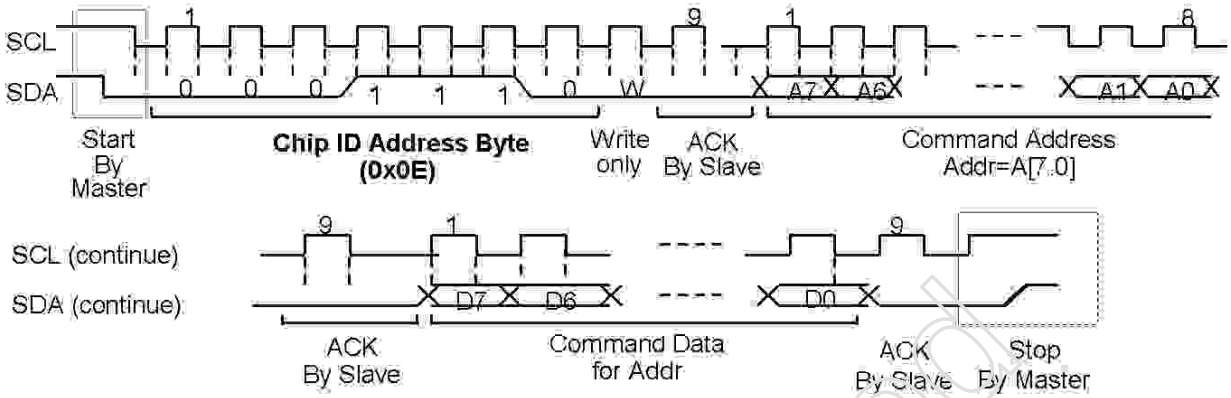
1. Devices that use non-standard supply voltages which do not conform to the intended I²C-bus system levels must relate their input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5$ V.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table 5 (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.36 without exceeding the maximum specified t_f.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

※ n/a = not applicable

❑ ASIC I²C Timing & Register Description

➢ Individual data Write mode of I2C control

※ Master: Image Board, Slave: PDP Module



✓ For "Write" function, first 1byte data should be **000 1110 (0)** ← last 1bit is 0(write mode)
✓ Start /Stop condition is generated by Master (=Image B'D).
✓ Before start condituon and/or after stop condition, SDA should not be recognized as a valid data.
✓ Start condition : SCL high & SDA transition from H to L.
✓ Stop condition : SCL high & SDA transition from L to H.

➢ I²C Register Brief

R : Reserved(don't care)

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x07	Bright Mode Registers							
	R	R	R	R	50av(2)	60av(2)	50PC(2)	60PC(2)
0x08	Bright Mode Registers							
	br_mode_50av (1:0)		br_mode_60av (1:0)		br_mode_50PC(1:0)		br_mode60PC(1:0)	
0x09	Power Save Mode Registers							
	R	R	ps_mode_50av (2:0)			ps_mode_60av (2:0)		
0x0A	Power Save Mode Registers							
	R	R	ps_mode_50PC(2:0)			ps_mode_60PC(2:0)		
0x10	Color Inversion Registers							
	R	R	R	R	R	R	R	Bw_inv_sw
0x18	ISM Mode Registers							
	R	R	R	R	R	ism_mode	1	1
0x20	Pattern Generation Registers							
	R	R	0	auto_ pat_gen	R	R	R	R

❑ ASIC I²C Timing & Register Description (continued)

➢ Bright Mode Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x07	Bright Mode Registers							
	R	R	R	R	50av(2)	60av(2)	50PC(2)	60PC(2)
0x08	Bright Mode Registers							
	br_mode_50av(1:0)		br_mode_60av(1:0)		br_mode_50PC(1:0)		br_mode60PC(1:0)	
Default	0	0	0	0	0	0	0	0

- br_mode_50av (2:0) : Bright mode for 50Hz and AV mode
- br_mode_60av (2:0) : Bright mode for 60Hz and AV mode
- br_mode_50PC(2:0) : Bright mode for 50Hz and PC mode
- br_mode_60PC(2:0) : Bright mode for 60Hz and PCmode

➢ Power Save Mode Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x09	Power Save Mode Registers							
	R	R	ps_mode_50av(2:0)			ps_mode_60av(2:0)		
0x0A	R	R	ps_mode_50PC(2:0)			ps_mode_60PC(2:0)		
Default	R	R	0	0	0	0	0	0

- Power Save Mode : The power consumption is controlled by varying the number of sustain.
- ps_mode_50av(2:0) : Power save mode for 50Hz and AV mode
- ps_mode_60av(2:0) : Power save mode for 60Hz and AV mode
- ps_mode_50PC(2:0) : Power save mode for 50Hz and PC mode
- ps_mode_60PC(2:0) : Power save mode for 60Hz and PC mode

※ Precautions when selecting Power Save Mode and Bright Mode

- Standard mode (AV mode)

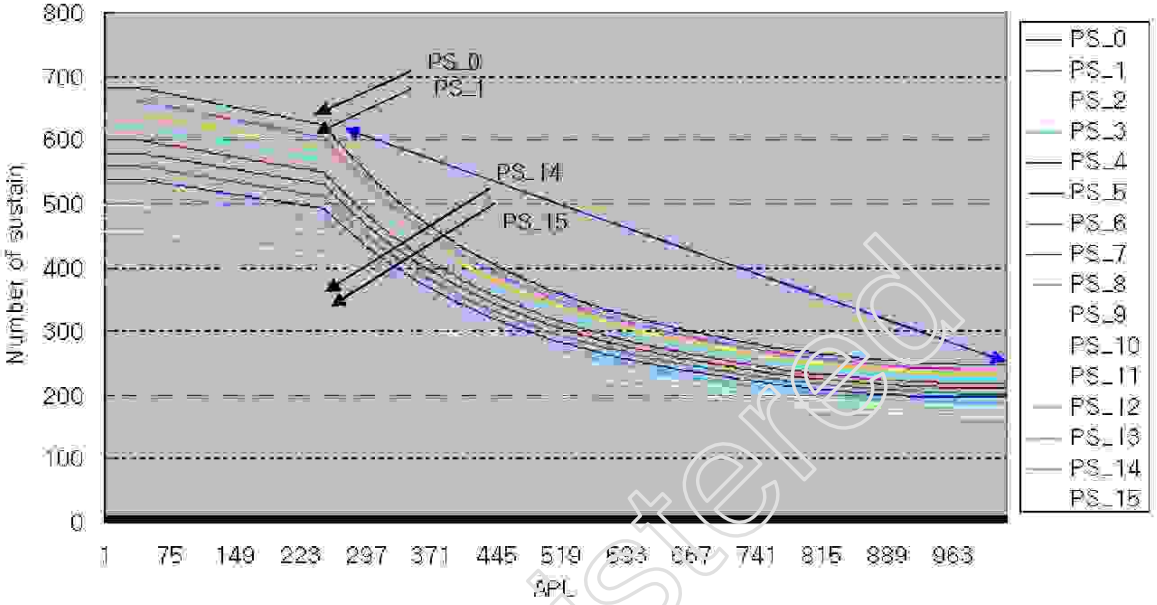
- Pen-touch mode (PC mode)

Please check model name, Pen-touch model or Standard model!

❑ ASIC I²C Timing & Register Description (continued)

➢ Standard Mode

* At Linear mode, unable Bright mode



* Possible use of combine Power save mode & Bright mode

Power Save Mode →

Bright Mode ↓

	P0	P1	P2	P3	P4	P5	P6
B0	Step 0 (PS_0)	-	-	-	-	-	-
B3	Step 1 (PS_1)	Step 2 (PS_2)	Step 3 (PS_3)	Step 4 (PS_4)	Step 5 (PS_5)	Step 6 (PS_6)	Step 7 (PS_7)
B4	Step 8 (PS_8)	Step 9 (PS_9)	Step 10 (PS_10)	Step 11 (PS_11)	Step 12 (PS_12)		

※ Each Step level is same value about 12 level Power consumption, Low/High temperature work 2 level of each Step

※ PS_0 ~ PS_12 : SVC UI

➢ Color Inversion Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x10	Color Inversion Registers							
	R	R	R	R	R	R	R	Bw_inv_sw
Default	R	R	R	R	R	R	R	0

• Image inversion enable signal for preventing image sticking
• bw_inv_sw : picture Color Inversion (1:ON, 0:OFF)

❑ ASIC I²C Timing & Register Description (continued)

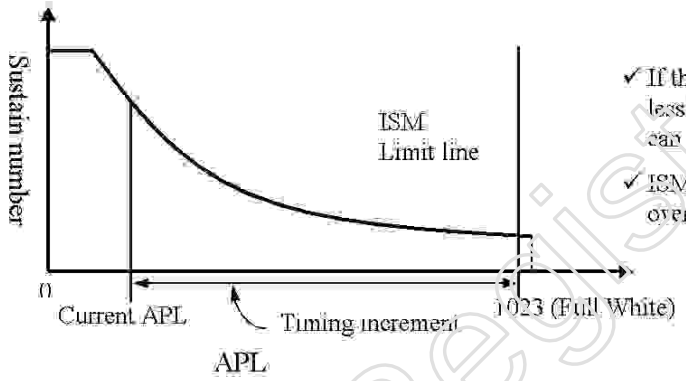
➢ ISM Mode Registers

▷ Image Sticking Minimization Method

ISM_CTRL, BWINV and SCROLL are all Image Sticking Minimization methods.
Two/three of them can be activated at a time, because they operate independently.

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x18	ISM Mode Registers							
	R	R	R	R	R	ism_mode	1	1
Default	R	R	R	R	R	1	1	1

• ims_mode : ISM mode switch (1 : ON, 0:OFF)



✓ If there is no movement (APL data variation is less than ± 5) for 5min. approximately, the brightness can be fallen near to Full White level

✓ ISM mode doesn't activated when APL is over the ISM limit line.

➢ Pattern Generation Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x20	Pattern Generation Registers							
	R	R	0	auto_ pat_gen	R	R	R	R
Default	R	R	0	0	R	R	R	R

• pat_auto_gen : Automatically pattern generation mode switch, 0:OFF, 1:ON
• automatically generated pattern sequence

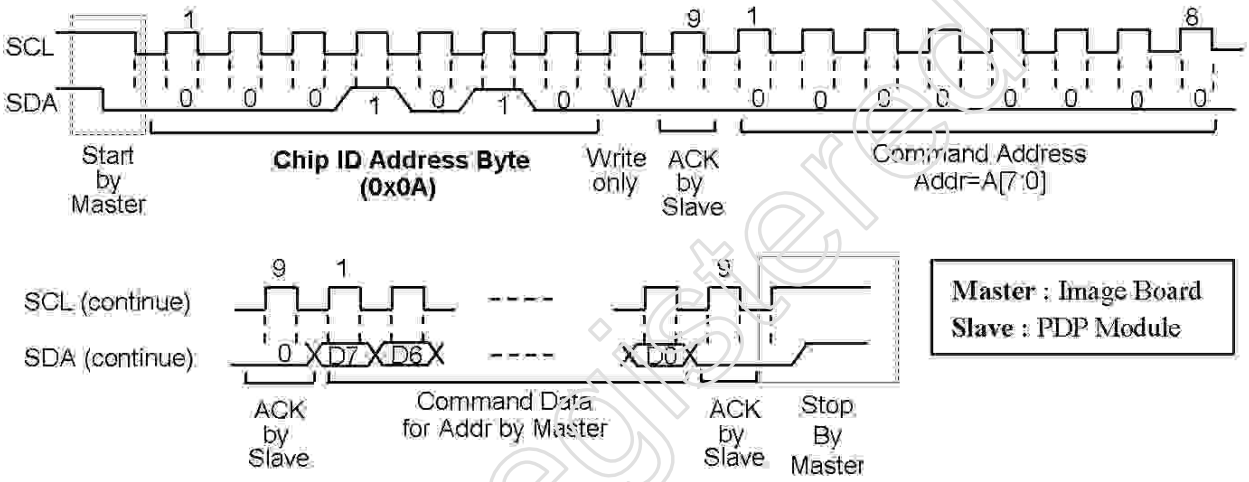
1) 1 pixel with fore-ground color at the start coordinate
2) full window with foreground
3) Peak window with X-Y coordinates
4) Life Pattern
5) 9 point box
6) 5 point box for testing the load effect
7) color bar
8) cross bar
9) gray level with 32*32 rectangular
10) vertical gray bar, 256 level
11) horizontal gray bar, 256 level
12) box window
13) horizontally scrolling the vertical gray bar
14) vertically scrolling the horizontal gray bar
15) horizontally moving the vertical bar
16) vertically moving the horizontal bar
17) Random Pattern

❑ FPGA I²C Timing & Register Description

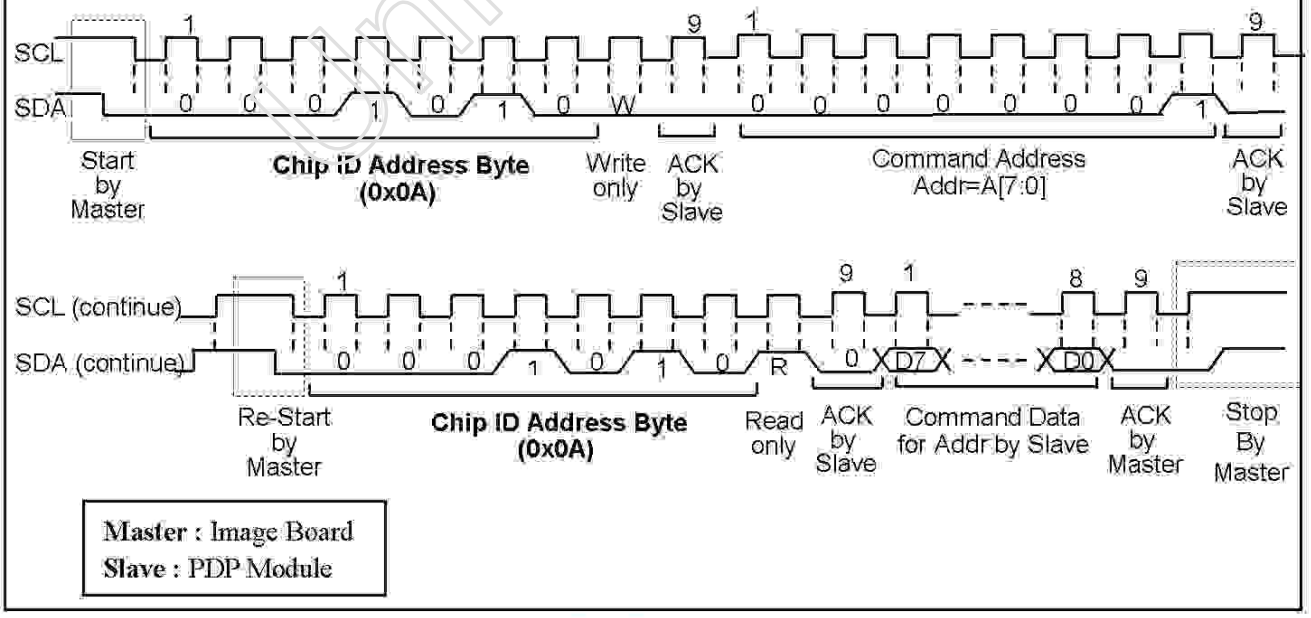
➢ I2C Register Map (Chip ID : 0A)

No	Item	Start Address	End Address	Description
1	APL module ID	0x10	0x10	APL module ID (Read only)
2	ISC Control	0xC1	0xC9,0xCF	ISC control

➢ Individual data write mode of I2C control (Chip ID : 0A)



➢ Individual data read mode of I2C control (Chip ID : 0A)



❑ FPGA I²C Timing & Register Description (continued)

➢ APL Module ID **(Read only)**

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x10	0	APL(6)	APL(5)	APL(4)	APL(3)	APL(2)	APL(1)	APL(0)

•APL Module ID (0~127) 6 5 4 3 2 1 0
MSB LSB

※ This is 'read only mode'. This express Control Board Dip Switch.

➢ ISC (Image Sticking Compensation) ON-OFF

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0xC1	0	0	0	0	0	0	0	ISC

•ISC : '1' - ON '0' - OFF

➢ ISC (Image Sticking Compensation) Curve selection

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0xC2	Red[1]	Red[0]	0	Green[1]	Green[0]	0	Blue[1]	Blue[0]

- Red [1:0] : Red Curve 0~3
- Green [1:0] : Green Curve 0~3
- Blue [1:0] : Blue Curve 0~3

➢ ISC (Image Sticking Compensation) Curve Calibration

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0xC3	Sign	0	0	0	0	0	Calibration_R_gain(9:8)	
0xC4	Calibration_R_gain(7:0)							
0xC5	Sign	0	0	0	0	0	Calibration_G_gain(9:8)	
0xC6	Calibration_G_gain(7:0)							
0xC7	Sign	X	X	0	0	0	Calibration_B_gain(9:8)	
0xC8	Calibration_B_gain(7:0)							

- Sign : '0' - '+' / '1' – '-'
- Calibration_R_gain[9:0] : Calibration ISC Curve Red / -1023~1023
- Calibration_G_gain[9:0] : Calibration ISC Curve Green / -1023~1023
- Calibration_B_gain[9:0] : Calibration ISC Curve Blue / -1023~1023

❑ FPGA I²C Timing & Register Description (continued)

➢ ISC (Image Sticking Compensation) pattern for ISC Curve Calibration

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0xC9	ON/OFF	0	0	0	0	0	Pet[1]	Pet[0]

•ON/OFF : '1' - ON '0' - OFF

•Pet[1:0] : 00 – F/W , 01- Red, 10 – Green , 11- Blue

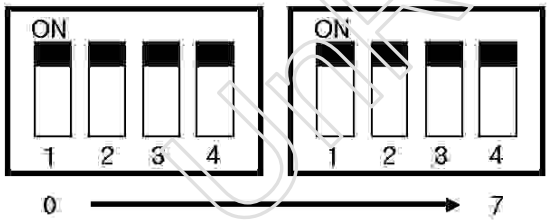
※ For pattern action, regular timing signal must be input into LVDS.
(Pattern is generated by external LVDS timing)

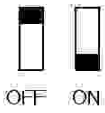
➢ ISC (Image Sticking Compensation) information Write (Write only)

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0xCF	0	0	0	0	0	0	0	0

※ Save I2C data for ISC control at memory (0xC1 ~ 0xC8)
Data will be remained at Power Off

❑ Control Board Dip Switch Description





Switch							
0	1	2	3	4	5	6	7
APL(0)	APL(1)	APL(2)	APL(3)	APL(4)	APL(5)	APL(6)	Pin_Sel

➢ APL Module ID

•APL Module ID : (0~127) **APL(0) APL(1) APL(2) APL(3) APL(4) APL(5) APL(6)**
LSB MSB

➢ PC Control I²C connector

•**Pin_Sel** : ON – PC Control I²C enable & Image board I²C disable
OFF - PC Control I²C disable & Image board I²C enable

3. ELECTRO OPTICAL SPECIFICATIONS

❑ Electro Optical characteristic Specifications (60Hz, with Filter)

ITEM			Symbol	Condition ☞1)	Min	Typ	Max	Unit
Peak White Brightness*			B_{WP}	1% white window	520	650	-	cd/m² ☞2)
Average White Brightness* ☞4)			B_W	Full White	56	66	-	cd/m²
Brightness Uniformity			B_U		-10	0	+10	%
Color Coordinate	White	X	X_W		0.285	0.295	0.305	
		Y	Y_W		0.300	0.310	0.320	
Color Coordinate Uniformity			C_U		-0.01	average	+0.01	
Contrast Ratio*	Bright Room		CR_{BR}	100Lx at center	-	125:1	-	☞2)
	Dark Room ☞3)		CR_{DR}	1% white window		1M:1	-	
Power Consumption			P_W	Full White	-	450	550	W

☞*) Module brightness can be lowed up to 25% comparing with room temperature when panel temperature is below than 18℃.

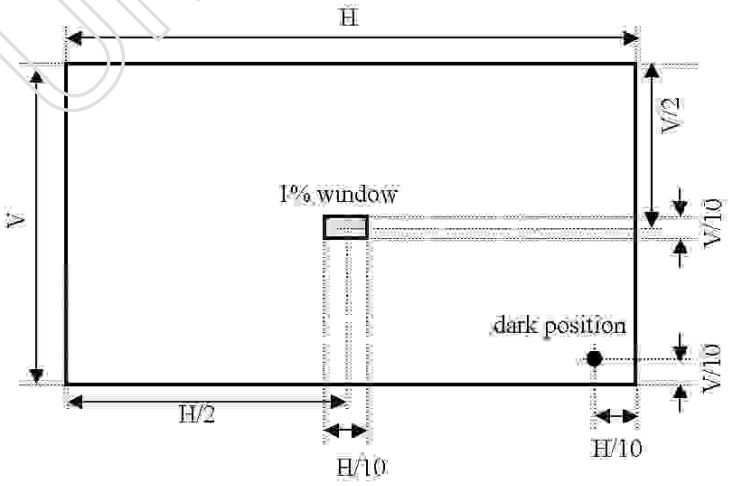
☞1) All characteristics are measured in the room temperature.

☞2) The brightness of the white peak position is measured while the 1%-window pattern is "ON" state. And then, it should be checked in 10 seconds after 1%-window is "ON" state

➔ Occasionally, the dark position could be changed to any other point arbitrary.

☞3) The brightness of dark room is less than 1 lux.

☞4) Average White Brightness is based on subsequent adjustments of White balance.

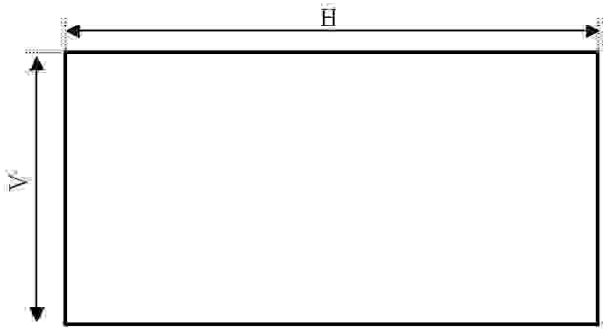


❑ Cell Defect Specifications

Defect	Specification	
	Number of Cell Defects (N)	Distance between two defects (D)
Non-Ignition Dot☞1) + Unstable Dot ☞2)	▶ Total N ≤ 12 [cells / full screen] ▶ N ≤ 12 [adjacency of3-cells / full-white screen] ≤ 0 [adjacency of 4-cells / full-white screen]	D ≤ 100mm, N ≤2 (100mm Circle/screen: 2points allowed)
Uncontrollable Dot ☞3)	▶ Total N ≤ 3 [cells / full screen]	
Non-Extinguishing Dot ☞4)	▶ N = 0	
▶ Total sum of all defects N ≤ 15 [cells / full-white screen]		
Stain ☞5)	▶ N ≤ 6 , for the stain of which longer-axis length is 5mm or shorter. ▶ N = 0 , for the stain of which longer-axis length is longer than 5mm.	▶ D ≥ 50 mm

☞1) Non-Ignition Dot(Dark Defect) is defined as "A cell of which more than 50% area is not ignited"
☞2) Unstable Dot (Flickering) is defined as "A cell which repeats On and Off"
☞3) Uncontrollable Dot is defined as "A cell which is distinctly brighter or darker than other cells around it" and/or "A cell of which color is distinctly different from that of other cells around it"
☞4) Non-Extinguishing Dot (brightness defect) is defined as "A cell of which more than 50% area is always ON"
☞5) Stain is defined as "A blob due to local color contamination in white or simple color pattern"

* The decision distance is 3H away from the panel, intensity of illumination is between 100 Lux and 200 Lux.
* Sensory stains and mis discharges are judged by IEC Interanational standard video pattern.



4. MECHANICAL & ENVIRONMENTAL SPECIFICATIONS

❑ Mechanical Characteristic Specifications

Item		Spec.	Unit	Remark
Outline Dimensions		1322.3(H) x 745.7(V) x 67.7(D) ±1	mm	See "Outline Drawing"
Display Area		1318.6 (H) × 741.9 (V) ± 0.5	mm	
Weight	Net	24.2 ± 1.0 (1EA) : with PSU	kg	
	Gross	247.8 ± 5 (8EA/1BOX) : with PSU	kg	

❑ Vibration and Drop Specifications

Item	Condition	Remark
Vibration	▶ 2Hz to 200Hz, Random 30min X, Y Direction, 1.04G(RMS) Z Direction, 0.73G(RMS)	▶ Non operation
Drop	▶ Bottom : Free falling : 20cm	

❑ Scratch and Dent Specifications

Item	Spec.	Unit	Remark
Scratch	W ≤ 0.01 ignored 0.01≤ W ≤ 0.09, 0.3≤ L≤25.4, N ≤ 1 0.1 ≤ W ≤0.14, L ≤12.7, N ≤ 1 0.14 < W, N = 0	mm	W : Width L : Length D : Depth N : Number
Dent	D ≤ 0.75, N ≤ 6	mm	

❑ Recommended Environmental Conditions

Item		Condition	Remark
Ambient Temperature	Operation	0℃to 60℃	
	Storage	-20℃ to 60℃	
Panel Surface Temperature	Absolute maximum temperature : 120 ℃(△T : ≤ 20 ℃/cm)		
Humidity	Operation	20 to 80% RH	No condensation
	Storage	10 to 90% RH	
Air Pressure	Operation	800 to 1,100 hPa	0~2000m above the sea level
	Storage	700 to 1,100 hPa	0~3000m above the sea level

5. IMAGE STICKING CHARACTERISTICS

❑ Image Sticking

The fluorescent substance used in the plasma module loses its brightness with the lapse of lighting time. This deterioration in brightness appears to be a difference in brightness in relation to the surroundings, and comes to be recognized as image sticking.

In other words, the image sticking is defined as follows: when the same pattern (of the fixed display) is displayed for a long time, a difference in brightness is caused around the lighting area and non-lighting area due to deterioration in the fluorescent substance.

When the present pattern is changed over to another one, the boundary comes to be seen between the lighting area and non-lighting area due to difference in brightness in the pattern shown shortly before changeover. If this conditions is accumulated, the boundary or image sticking comes to be seen with the naked eyes.

❑ Secular change in brightness

The life of brightness, defined as the reduction to half the initial level, is more than 60 thousand hours on average.

Conditions: All white (100% white) input at an ambient temperature of 25°C.

However, this lifetime is not a guarantee value for life and brightness, it should be recognized simply as the data for reference.

❑ Warranty

Image sticking and faults in brightness and picture elements are excluded from the warranty objects.

❑ Cause of deterioration in brightness

A major possible cause of deterioration in brightness is damage in the fluorescent substance due to impact caused by ions generated at the time of plasma discharges.

❑ Practical value for image sticking

The relationship between integrated lighting time and brightness in this plasma module is described in the attached material. In particular, the deterioration in brightness tends to be accelerated up to 100 hours in the initial period. In the initial period, the fixed display of patterns particularly tends to cause image sticking. The practical value for image sticking is difficult in concrete numerals. As described below, you are advised to take proper measures to make the occurrence of image sticking as slow as possible.

❑ Proposed measures taken to relieve image sticking

So long as there is the reduction of brightness in the fluorescent substance, it is impossible to avoid the occurrence of image sticking. Therefore, to relieve image sticking, we offer you a method of entering an image input that may ensure reluctance to the generation of the difference in brightness reduction among the displayed dots

The images from TV broadcasting involve a high rate of motion picture displays. Therefore, there is less chance of being a cause of difference in brightness reduction among the cells. Even when the fixed patterns are displayed, they generally last for a few minutes. Since the same pattern is less liable to be displayed, there is almost no influence toward image sticking.

If the fixed patterns tend to be displayed for a long time, however, there occurs a substantial imbalance between the lighting and non-lighting areas, thus causing a difference in brightness as a result. In this document, we offer you some proposals of installation, paying attentions to the two points, the reduction of difference in brightness achieved by integrated lighting time leveling and the method of edge smearing to make image sticking hard to be discerned.

The result from these proposals can, however, greatly depend on the contents of images and the operating environment. Therefore, we consider that it is essential to take the suitable measures in consideration of the customer's operating environment.

Example of Proposal 1: The display position is moved while the fixed display pattern is changed over, or it is scrolled during the display.

Example of Proposal 2: If possible, a pattern of complementary color is incorporated (for integrated time leveling).

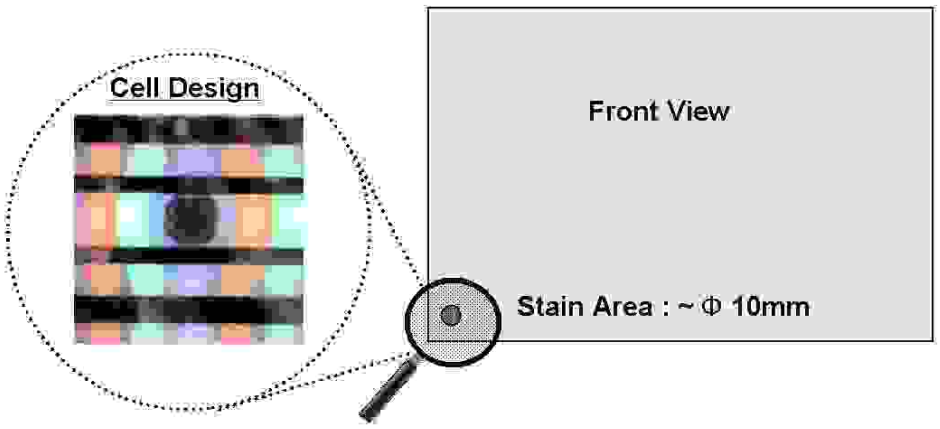
Example of Proposal 3: The fixed pattern and the motion picture display are reciprocally exchanged, in order to minimize display period of the fixed pattern.

Example of Proposal 4: During operation, the brightness of screen is suppressed as low as possible. For the display patterns, characters are indicated not on the black ground (non-picture area) but on the colored ground (mixture of R, G, B recommended).

6. Stain of Exhast Hole

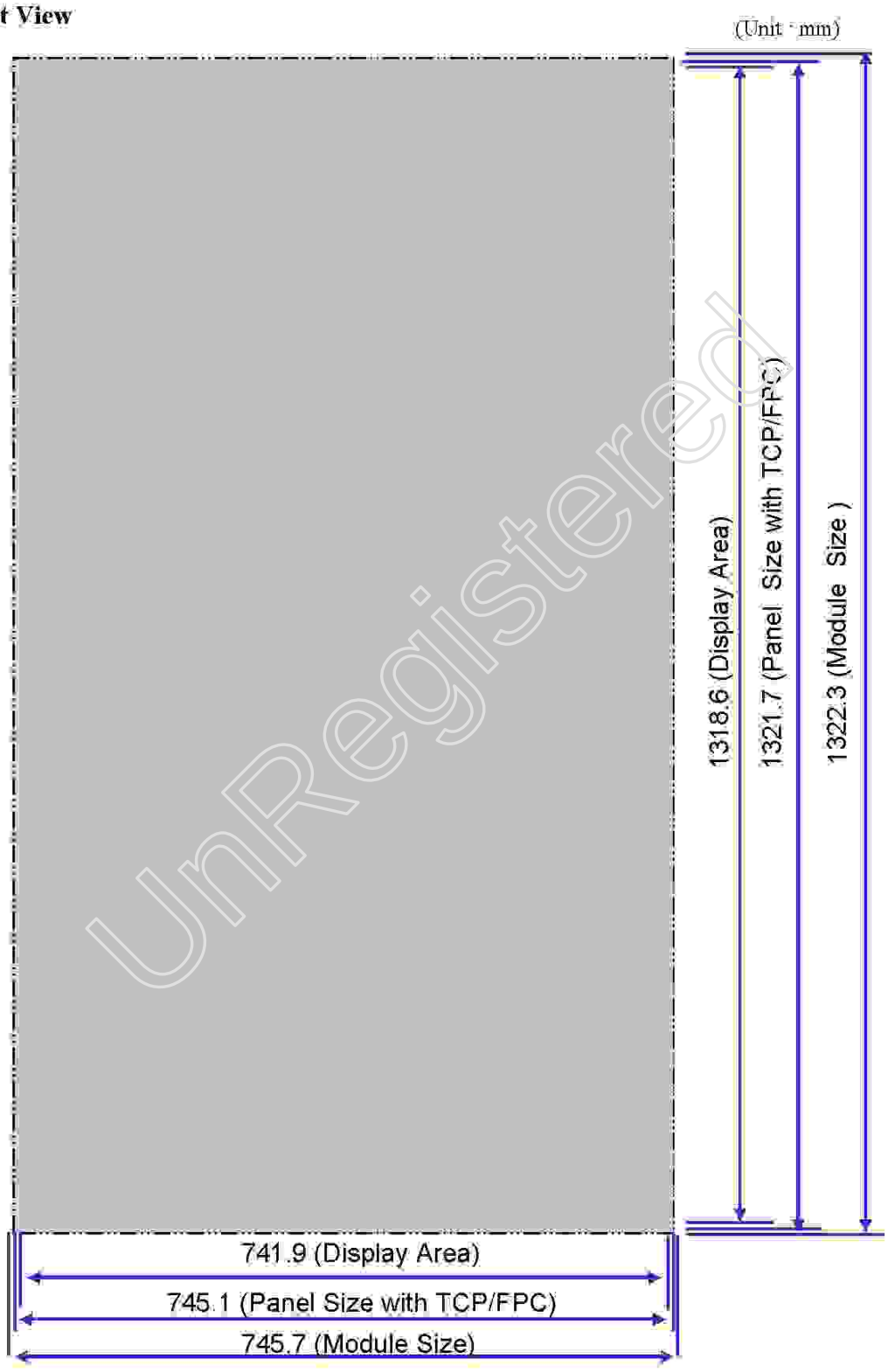
Though Brightness uniformity meets the Optical Specification, it may be possible for the stain or misdischarge to be seen in some areas in the bottom corner on a given video signal.

It is characteristics of the model that the lag appears as the exhaust hole should be moved into active areas to minimize the seam size in commercial multi PDP model.



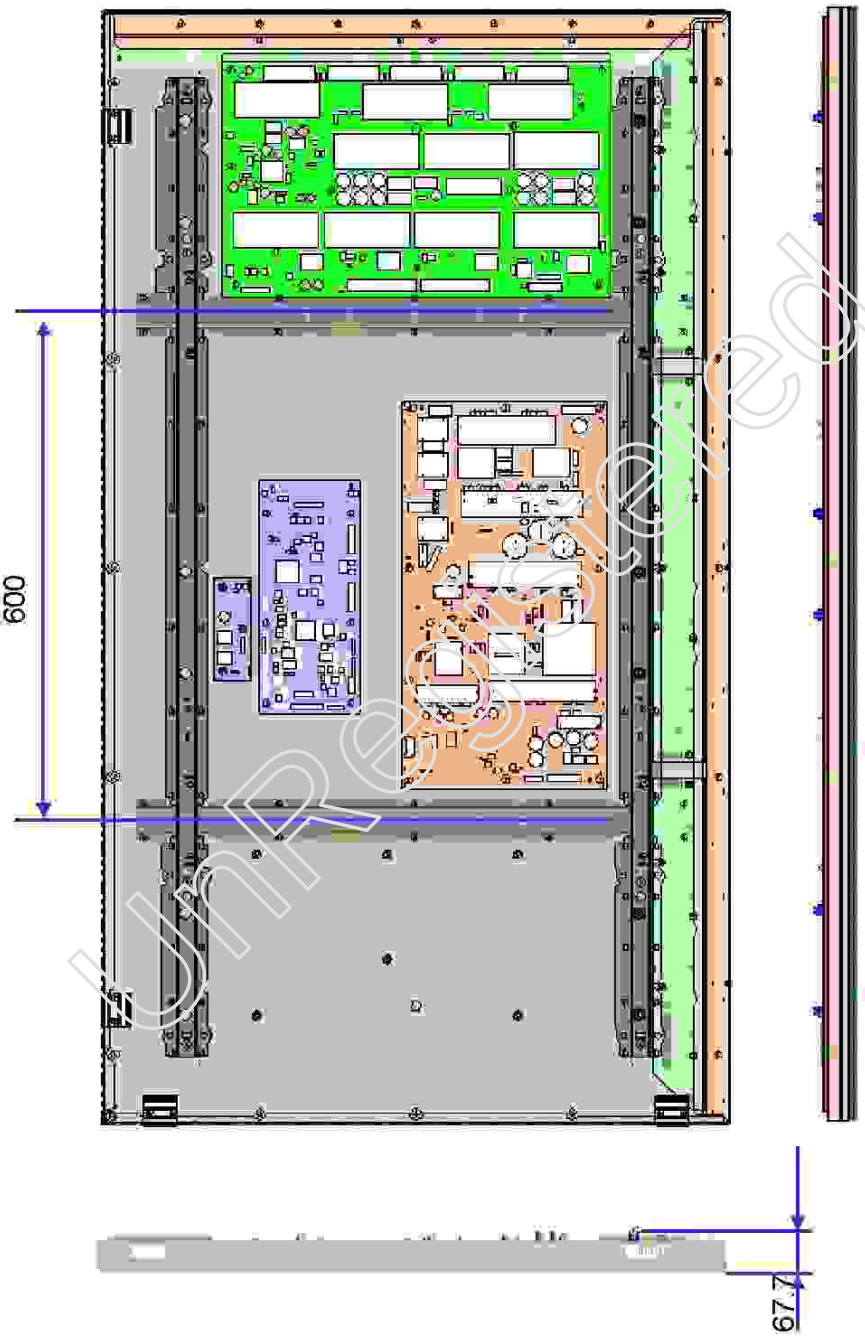
6. OUTLINE DRAWING

❑ **Front View**



❑ Rear View

(Unit : mm)



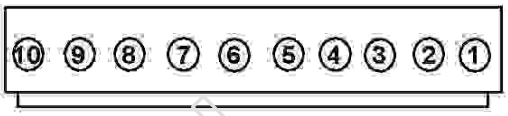
7. CONNECTORS and CONNECTIONS

❑ Power Input Connector

➢ Connector Pin Assignment (Y SUS Board : P200)

Pin No	Symbol	Pin No	Symbol
1	Vs	6	Va
2	Vs	7	Va
3	NC	8	GND
4	GND	9	5V
5	GND	10	5V

YAW396 – 103V Pin numbers
(View from the pin connection side)

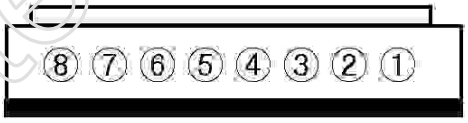


Connector : YAW396 - 103V
Housing : YH396 - 10V
Maker : Yeonho

➢ Connector Pin Assignment (CTRL Board : P502)

Pin No.	Symbol	Pin No.	Symbol
1	5V	5	GND
2	5V	6	GND
3	5V	7	GND
4	5V	8	GND

GT200-08P-SS-A Pin numbers
(Top View)

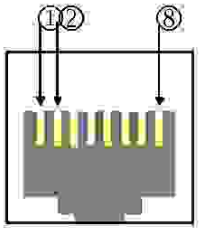


Connector : GT200-08P-SS-A
Housing : GIL-S-8S-S2C2-S
Maker : LS Cable,Yeonho

❑ Modular Jack

To make same brightness for each module in multi-PDP system.

Communication among modules – sharing APL information.



➢ Connector Pin Assignment (CTRL Board)

P602 : RX

Pin No.	Symbol	Pin No	Symbol
1	Rx_CLK	5	GND
2	GND	6	GND
3	Rx_DATA	7	Rx_nDE
4	GND	8	GND

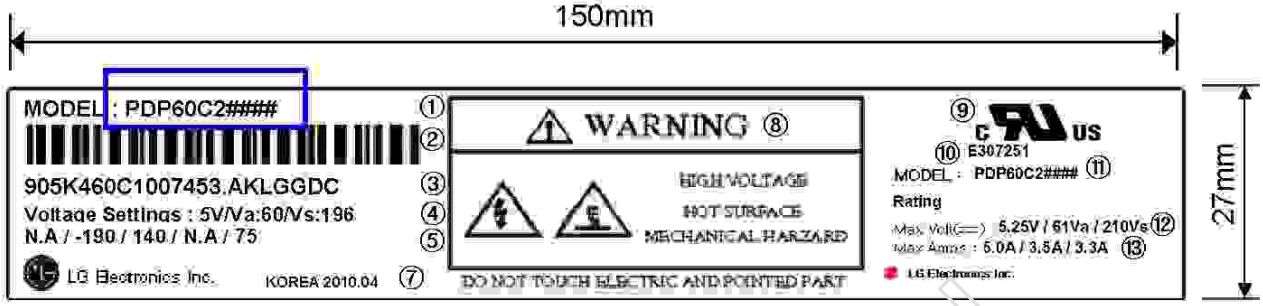
P601 : TX

Pin No.	Symbol	Pin No.	Symbol
1	Tx_CLK	5	GND
2	GND	6	GND
3	Tx_DATA	7	Tx_nDE
4	GND	8	GND

RV1-1000000A (maker : UDE)

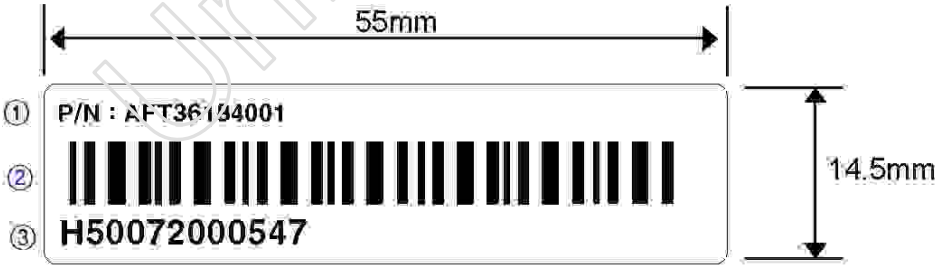
8. Label

❑ Unification Label

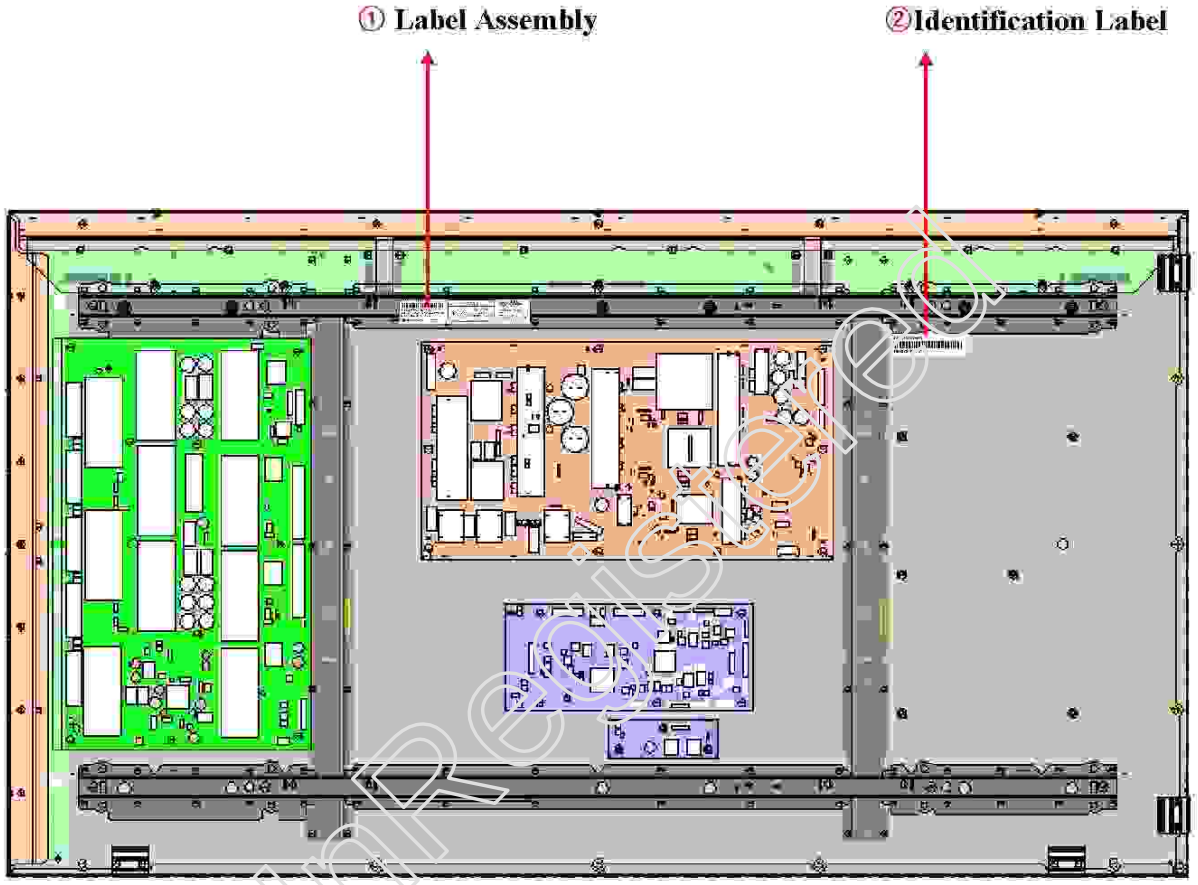


① Model Name
② Bar Code (Code 128, Contains the manufacture No.)
③ Manufacture No.
④ Adjusting Voltage (DC Va, Vs)
⑤ Adjusting Voltage (Set up/ -Vy/ Vsc/ Ve/ Vzb)
⑥ The trade name of LG Electronics
⑦ Manufactured date (Year & Month)
⑧ Warning
⑨ UL Approval Mark
⑩ UL Approval No.
⑪ Model Name
⑫ Max. Volts
⑬ Max. Amps

❑ Module ID Label

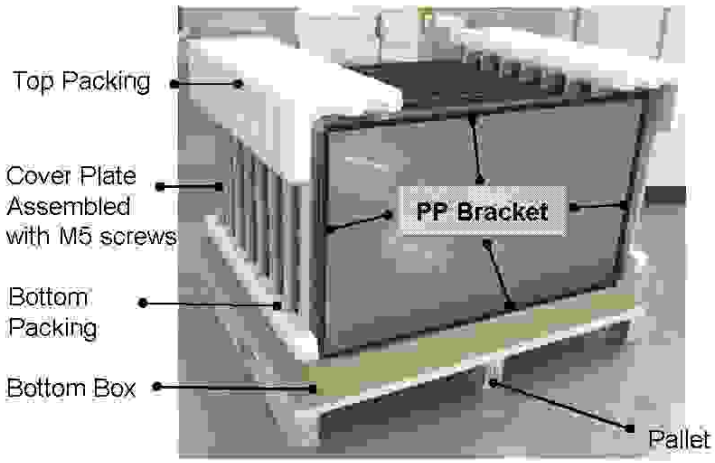


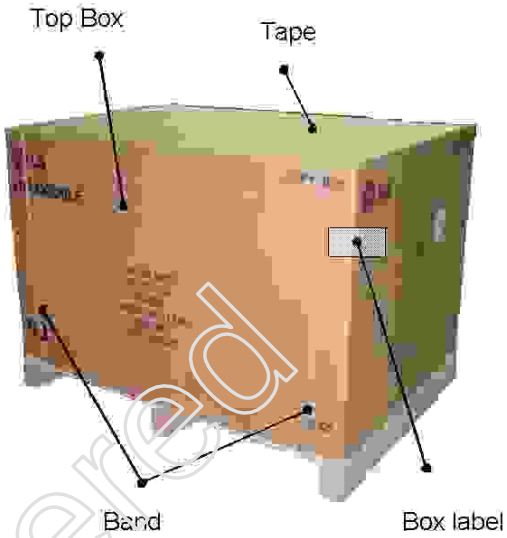
① Module frame ass'y part number
② Bar Code Containing the manufacture No.
③ Manufacture No.



9. PACKING

❑ Box packing (8 modules per each Box)

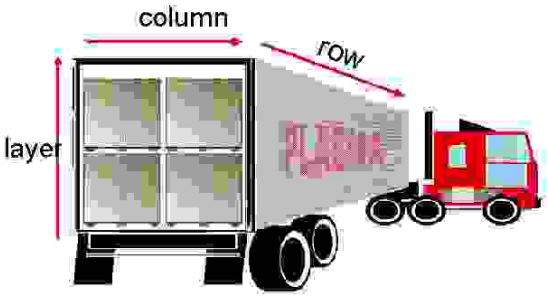
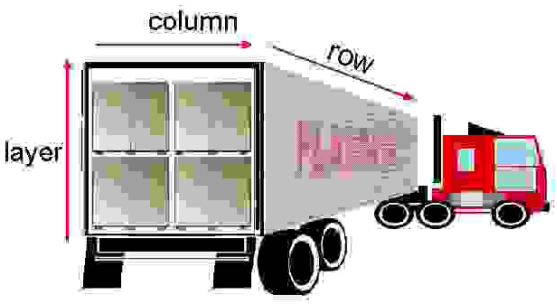




※ Caution

-. 'PP Bracket' is only used to protect the edge of panel.
If you used that another purpose, you have all responsibility for following results.
-. Set-up the multi-vision, after removing 'PP Bracket'.
-. Clean the remained adhesive on the module after removing 'PP Bracket'.

❑ Quantity on Container

40 feet Container	20 feet Container
7*2*2 (28Box)	3*2*2 (12Box)
	

❑ Caution for handling of the module package

1. Packing Movement, Loading & Keeping
- Left & right Direction of Module should be matched with direction of fork-lift truck.
- When fork-lift truck is moving into direction of module's front and rear,
  Prevent accelerating and decelerating rapidly.
- It can be loaded two layer boxes and should be keeped in a warehouse.
- The storehouse must maintain dehumidification state and the same temperature all the time.

2. Fork-Lift Truck Loading
- When module boxes are loaded in a car, their direction should be matched the same of fork-lift truck
- Spare packing (under 7ea) should be loaded at last top in a car and Quantity
  should be written at box.
- The end of container, sealing with packing, should be prevented slipping during the transportation.